https://stanfordgroup.org/

Biomedical and Pharmacological Literature Archives

Vol 5, Issue 2, 2025

DESIGN AND ANALYSIS OF 8-BIT MULTIPLIER FOR LOW POWER VLSI APPLICATIONS

Mrs. L. GAVIRAMMA[1], S.V.SRI LAKSHMI[2], G. RISHIKA[3]

[1]Assistant Professor, Dept. of ECE, PRAGATI ENGINEERING COLLEGE

[23]UG Students, Dept. of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

The multiplier stands as a fundamental component within the multiply and accumulate (MAC) unit, particularly prevalent in digital signal processing (DSP) applications. Traditionally, multiplication involves repeated addition, leading to extensive use of full adders (FAs) in the process. The energy efficiency of the multiplier is gauged by power delay per bit operation. Consequently, the efficiency of the multiplier hinges significantly on the role played by the full adder.

In this project conducts a comprehensive study, design, implementation and simulation of an 8-bit additive multiply module (AMM), employing diverse full adder circuit architectures. The designed AMM is then compared with traditional Wallace/Dadda tree multipliers across various design metrics. For the purpose of comparison, all multipliers are described using RTL codes, and the designs are simulated and verified using EDA tools.

INTRODUCTION

The fundamental blocks of multiply and accumulate circuits (MACs), namely the FA and multiplier circuits (FMCs), play a pivotal role in determining the overall performance of Digital Signal Processing (DSP) systems. These FMCs typically consume a substantial amount of power in any DSP-based system, necessitating the optimization of their performance for specific applications. In today's rapidly expanding realm of soft computing and digital technology, there is a burgeoning demand for power-efficient handheld devices. These devices, predominantly battery-operated, are tasked with processing computationally intensive operations.

A multitude of portable electronic devices, including cellular phones, iPods, laptops, and contemporary Internet of Things (IoT) devices, necessitate low power consumption without compromising performance. Among the components contributing to power consumption in

microprocessor Arithmetic Logic Units (ALUs), the multiplier stands out as a significant consumer. Lowering a device's power consumption can be addressed at various design levels, spanning logic, circuit, gate, and transistor levels. Accelerating partial product accumulation is imperative for enhancing multiplication speed, thereby improving overall system performance.

LITERATURE SURVEY

1.**"Low Power Multiplier Design Using Modified Full Adder"** by Kumar et al. (2015) This paper introduces a low-power multiplier design using a modified full adder structure. By optimizing the adder architecture, the proposed multiplier achieves significant power savings without compromising performance.

2. "Energy-Efficient Design of Approximate Multipliers for Error-Tolerant Applications" by Zhang et al. (2017) Zhang et al. propose an energy-efficient design methodology for approximate multipliers targeting error-tolerant applications. The study explores various approximation techniques and trade-offs between accuracy and power consumption.

3. "Low Power and Area Efficient 8×8-Bit Parallel Multiplier Design Using Hybrid CMOS and Adiabatic Logic" by Anand et al. (2018) Anand et al. present a novel approach to designing low-power and area-efficient 8×8-bit parallel multipliers by integrating hybrid CMOS and adiabatic logic techniques.

4. "Design of Low Power 8-Bit Multiplier Using Efficient Carry Select Adder and Multiplexer Based on MTCMOS Technique" by Reddy et al. (2019) Reddy et al. propose a novel 8-bit multiplier design strategy utilizing an efficient carry select adder and multiplexer based on the Multi-Threshold CMOS (MTCMOS) technique. By leveraging the advantages of MTCMOS for dynamic power management, the proposed multiplier achieves substantial reductions in power consumption while meeting performance requirements.

PROPOSED METHODOLOGY

Proposed Multiplication Using Amm (Additive Multiply Module)

The Additive Multiply Module (AMM) is a computational unit used in digital signal processing and arithmetic operations. It combines addition and multiplication operations within a unified

framework to efficiently compute products of two numbers. In the AMM, the multiplicand and multiplier are divided into segments, and each segment is multiplied independently. The partial products obtained from these multiplications are then added together to yield the final product.

This modular approach reduces the critical path delay and improves performance compared to conventional multiplier designs. Additionally, the AMM architecture is well-suited for low power VLSI applications due to its reduced switching activity and power consumption. By leveraging parallel processing and optimized algorithms, the AMM achieves high-speed multiplication while maintaining energy efficiency.

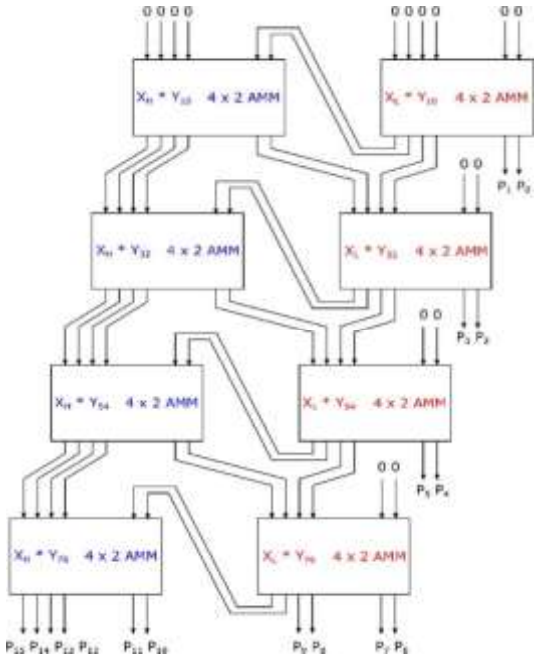


Figure.1 Block diagram of binary 8×8 AMM

SIMULATION & SYNTHESIS RESULTS

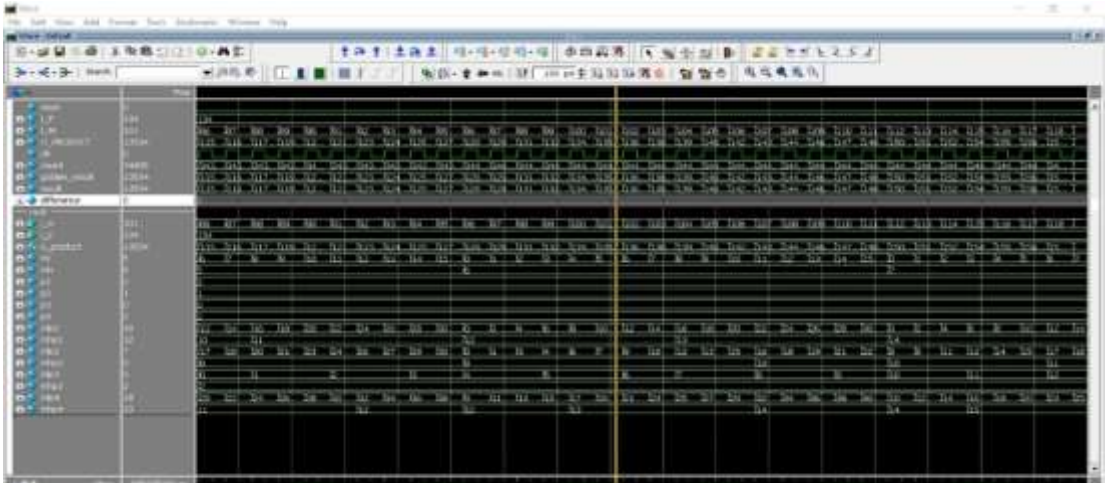


Figure.2 Simulation Results of 8-bit Multiplier using AMM

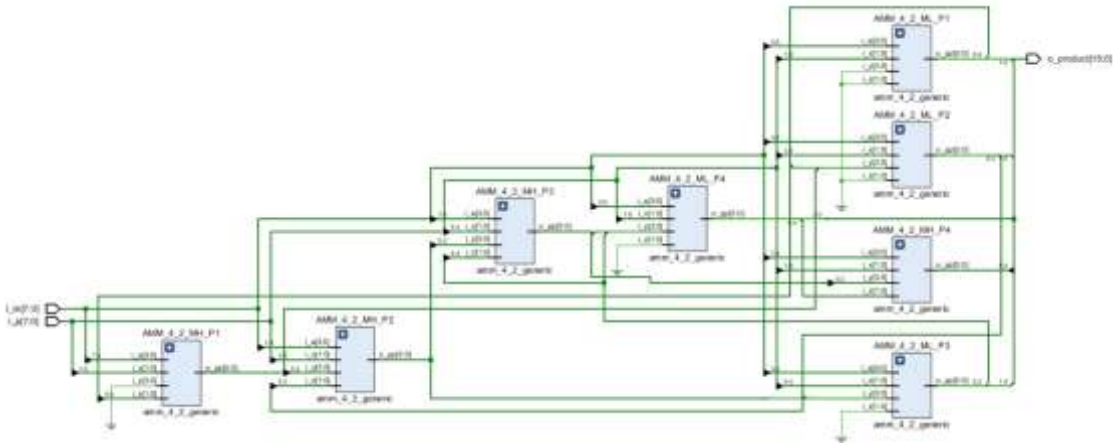


Figure.3 Schematic Diagram of 8-bit Multiplier

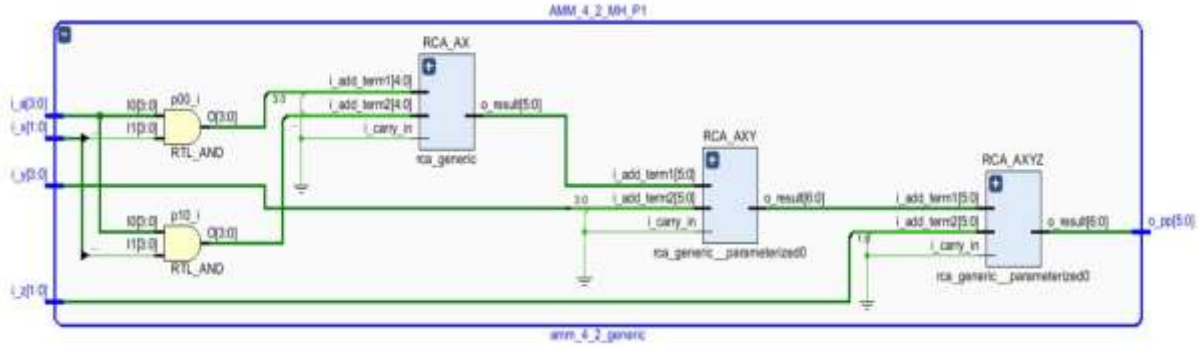
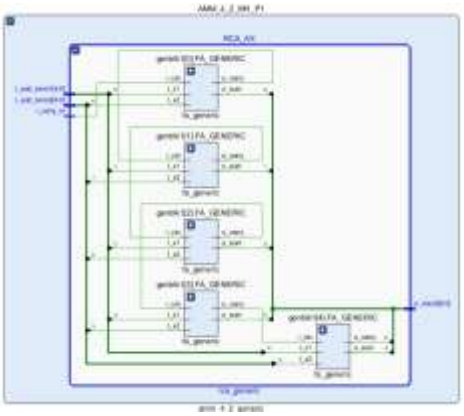


Figure.4 Schematic Diagram of AMM (Additive Multiply Module)



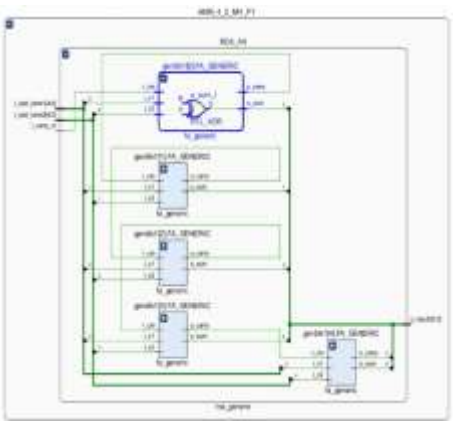


Figure.5 RCA (Ripple Carry Adder)

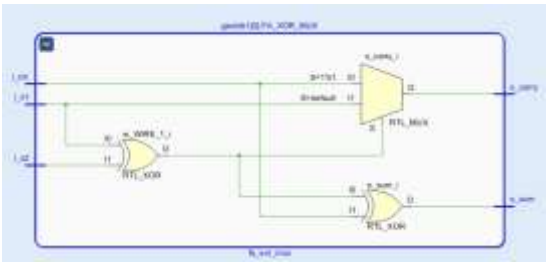


Figure.6 Generic Full Adder

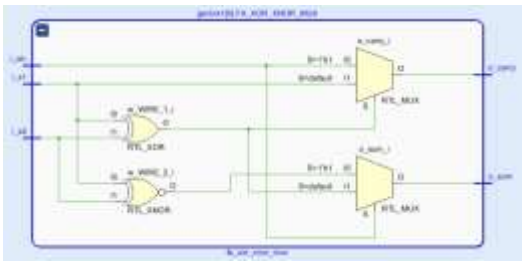


Figure.7 XOR Mux Full Adder

Figure.8 XNOR Mux Full Adder

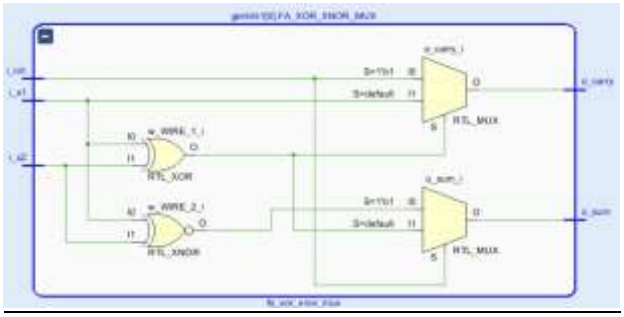


Figure.9 XOR/XNOR Mux Full Adder

Area Report Multiplier Generic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	110	0	303600	0.04
LUT as Logic	110	0	303600	0.04
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT6	80	LUT
LUT5	19	LUT
OBUF	16	IO
IBUF	16	IO
LUT2	14	LUT
LUT4	10	LUT
LUT3	8	LUT

Area Report Multiplier XNOR

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	105	0	303600	0.03
LUT as Logic	105	0	303600	0.03
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT6	67	LUT
LUT4	30	LUT
LUT5	20	LUT
OBUF	16	IO
IBUF	16	IO
LUT2	12	LUT
LUT3	2	LUT

Area Report Multiplier XOR

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	105	0	303600	0.03
LUT as Logic	105	0	303600	0.03
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT6	67	LUT
LUT4	30	LUT
LUT5	20	LUT
OBUF	16	IO
IBUF	16	IO
LUT2	12	LUT
LUT3	2	LUT

Area Report Multiplier XNOR-XOR

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	105	0	303600	0.03
LUT as Logic	105	0	303600	0.03
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT6	67	LUT
LUT4	30	LUT
LUT5	20	LUT
OBUF	16	IO
IBUF	16	IO
LUT2	12	LUT
LUT3	2	LUT

ADVANTAGES

- Enhanced Power Efficiency
- Optimized Architectural Design
- Streamlined Multiplication Process
- integration of Advanced Power Optimization Techniques

APPLICATIONS

Mobile Devices: Integration into smartphones, tablets, and smartwatches to enhance battery life and overall energy efficiency.

IoT Devices: Utilization in Internet of Things (IoT) devices such as sensors, actuators, and smart home appliances to prolong battery life and reduce power consumption.

Wearable Electronics: Incorporation into wearable devices like fitness trackers, health monitors, and augmented reality glasses for efficient data processing and extended battery runtime.

Portable Electronics: Integration into portable electronics such as handheld gaming consoles, digital cameras, and portable media players for power-efficient arithmetic operations.

Wireless Sensor Networks (WSNs): Incorporation into WSN nodes for efficient data processing, sensor fusion, and communication tasks, enabling long-term operation in remote and energy-constrained environments.

CONCLUSION

In conclusion, the project entailed the design and analysis of 8×8-bit multipliers employing Additive Multiply Module (AMM) architectures. Using Verilog RTL codes based on a generic Full Adder (FA) architecture, the multipliers were simulated and verified for functionality across various input data combinations. Additionally, the designs underwent synthesis for FPGA.

To further explore power efficiency, the multipliers were implemented with different FA architectures including XOR-Mux, XNOR-Mux, and XOR/XNOR-Mux. Comparative analysis was performed for FA architectures and conclude that AMM multiplier consumes less power compared to WTM and DTM, rendering it suitable for various low-power VLSI applications

FUTURE SCOPE

The future scope of this project involves exploring optimal formulas for partitioning Trunc signals to enhance performance. Further investigation will delve into analyzing various partition methods to establish clearer correlations between hardware costs, accuracy, and power consumption through concrete or mathematical expressions. Notably, our current study highlights the need for tailored Trunc signals across different networks or convolutional layers to achieve satisfactory outcomes with the proposed adjustable approximate multiplier. Future efforts will prioritize addressing this aspect to advance the effectiveness of the methodology.

REFERENCES

1.Nitin Krishna V, “Performance Analysis of MAC Unit using Booth, Wallace Tree, Array and Vedic multipliers,” International Journal of Engineering Research and Technology, Vol. 09, Issue 09,Sept. 2020.

2. C. V. Gowdar, M. C. Parameshwara and S. Sonoli, “Approximate Full Adders for Multimedia Processing Applications,” 2020 IEEE International Conference for Innovation in Technology (INOCON), 2020, pp. 1-4

3. Parameshwara, M.C., “Approximate full adders for energy efficient image processing applications" Journal of Circuits, Systems and Computers, vol. 30, issue 13, pp.1-17, Oct. 2021.

4. Jain, S. Bansal, S. Khan, S. Akhter and S. Chaturvedi, “Implementation of an Efficient N×N Multiplier Based on Vedic Mathematics and Booth-Wallace Tree Multiplier” 2019 International Conference on Power Electronics, Control and Automation (ICPECA), 2019, pp. 1-5.

5. Parameshwara, M.C., Nagabushanam, M. “ Novel low quantum cost reversible logic based full adders for DSP applications. " International Journal of Information Technology. 2021, vol. 13, pp.1755–1761.

6. P. Yadav, A. Pandey, M. R. K., R. P. K.J., V. M.H. and N. K.Y.B., “Low Power Approximate Multipliers with Truncated Carry Propagation for LSBs,” 2018 IEEE 61stInternational Midwest Symposium on Circuits and Systems (MWSCAS), pp. 500-503, 2018.