HIGHLY EFFICIENT MULTIPLIER DESIGN WITH ADJUSTABLE TRUNCATION FOR POWER SAVING

Mr. V. PRASANTH[1], PALUKURI ANUSHA[2], MASINIDI SUBRAHMANAYAM[3]

[1]Associate Professor, Dept. of ECE, PRAGATI ENGINEERING COLLEGE

[23]UG Students, Dept. of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

In various applications, multipliers play a crucial role, demanding substantial power consumption due to frequent multiplication operations. To address this, this Project propose an adjustable approximate multiplier that dynamically truncates partial products to balance accuracy, energy efficiency, and performance. Our approach includes a high-accuracy 4-2 compressor and a flexible error compensation circuit, allowing users to tailor accuracy and power consumption based on specific requirements at runtime. Experimental results showcase a notable reduction in delay and in average power consumption compared to the conventional Wallace tree multiplier

INTRODUCTION

The project centers around the development of a "Low-Power and High-Accuracy Approximate Multiplier with Reconfigurable Truncation." The need for approximate multiplication arises from the understanding that certain applications can tolerate a degree of error in exchange for substantial gains in power efficiency. This trade-off becomes particularly relevant in battery-powered devices, Internet of Things (IoT) applications, and other energy-constrained environments where power consumption is a critical concern.

The key innovation lies in the incorporation of reconfigurable truncation techniques, allowing dynamic adjustments to the precision of the multiplier based on the specific requirements of the application. This adaptability not only facilitates energy-efficient computations but also ensures that the accuracy of the results remains within acceptable bounds for the given context.

As technology continues to advance, the significance of energy-efficient designs becomes paramount. The proposed low-power approximate multiplier promises to contribute to this paradigm shift by offering a flexible solution that addresses the delicate balance between computational accuracy and power consumption. This project report aims to comprehensively detail the design methodology, implementation, and performance evaluation of the

aforementioned multiplier, shedding light on its potential applications and impact in modern computing sy stems.

LITERATURE SURVEY

1."Low-Power Approximate Multiplier Using Truncated Booth Encoding" (2015) This study explores the utilization of Truncated Booth Encoding to design a low-power approximate multiplier. It investigates methods to reduce power consumption while maintaining reasonable accuracy.

2. "High-Accuracy Approximate Multiplier Using Dynamic Approximate Radix-4 Booth Encoding" (2017) The research presents a high-accuracy approximate multiplier achieved through the implementation of Dynamic Approximate Radix-4 Booth Encoding. It focuses on enhancing accuracy without compromising on performance.

3. "Reconfigurable Approximate Multiplier Architecture for Energy-Efficient Signal Processing" (2019) This paper introduces a reconfigurable approximate multiplier architecture aimed at facilitating energy-efficient signal processing. It discusses methods to dynamically adjust the approximation level based on computational requirements.

4."A Comprehensive Survey of Approximate Multipliers and Its Impact on Digital Signal Processing" (2020) The survey provides an overview of various approximate multiplier designs and their impact on digital signal processing applications. It discusses the trade-offs between power consumption, accuracy, and performance.

5. "Energy-Efficient Approximate Multiplier Design Using Approximate Radix-2 Booth Encoding" (2022) This research investigates the design of an energy-efficient approximate multiplier utilizing Approximate Radix-2 Booth Encoding. It explores techniques to reduce energy consumption while maintaining acceptable accuracy levels.

PROPOSED SYSTEM

In this study, we introduce a 4-2 compressor with a focus on achieving high accuracy. Building upon this, we extend our design to create a high-accuracy approximate multiplier. Additionally, we present a novel dynamic input truncation technique, allowing for the adjustment of both accuracy and power consumption as needed.

The key contributions of this paper can be outlined as follows:

We present a high-accuracy approximate 4-2 compressor, providing a foundational element for constructing the proposed approximate multiplier.

Our paper introduces a dynamic input truncation technique, offering the flexibility to adjust both accuracy and power requirements in multiplication operations. This technique is particularly well-suited for Convolutional Neural Networks (CNNs), where power consumption can be easily tailored to the specific demands of each layer.

Leveraging the proposed 4-2 compressor, the error compensation circuit, and the dynamic input truncation technique, we put forth a high-accuracy and reconfigurable approximate multiplier. This comprehensive approach aims to provide a versatile solution that addresses both accuracy and power considerations in computational tasks.

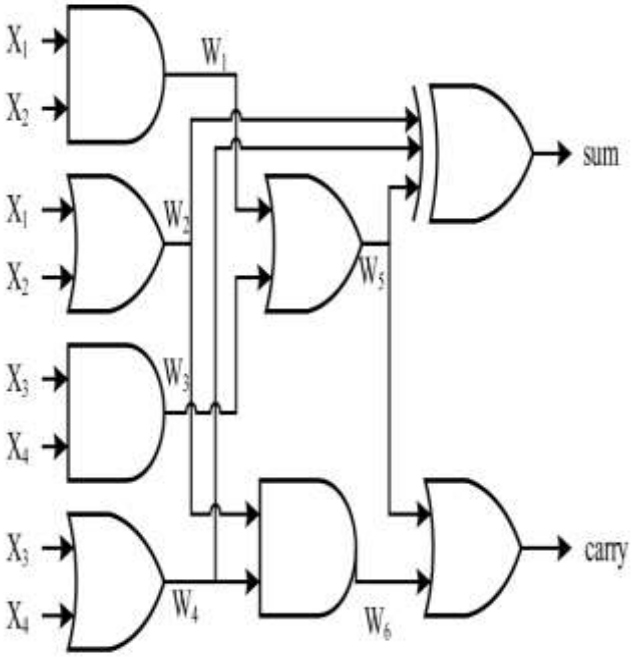

Figure.1 Schematic Diagram

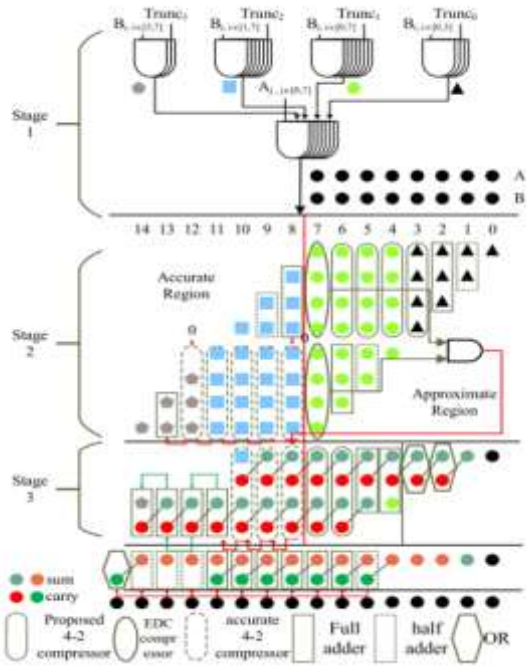

figure.2 Proposed Approximate Multiplier

SIMULATION & SYNTHESIS RESULTS

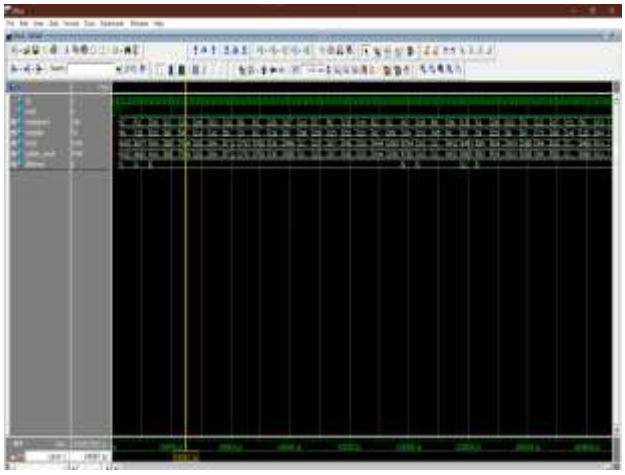

Figure.3 Simulation output1

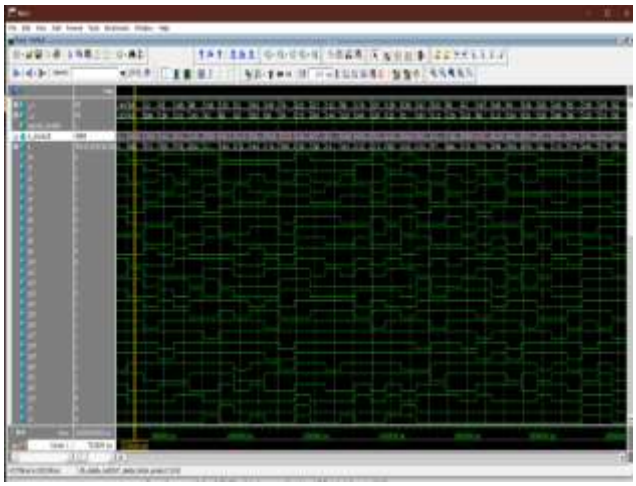

Figure.4 Stimulation output2

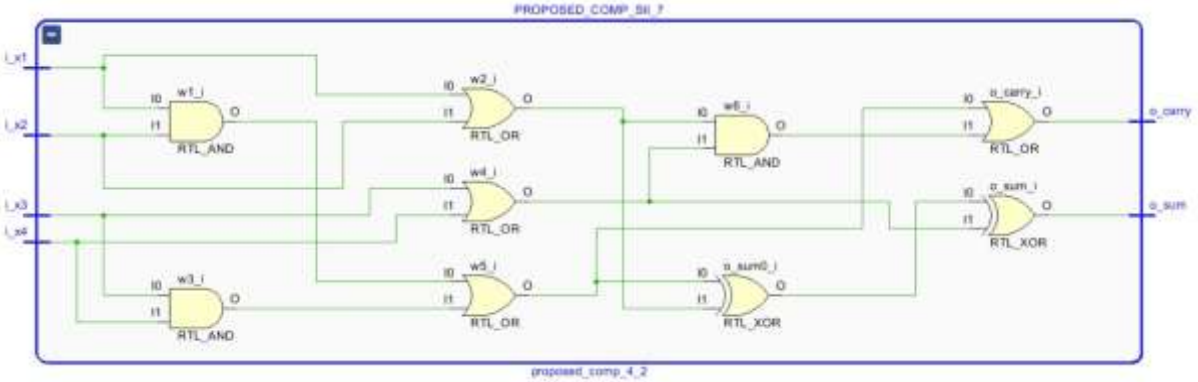

Figure.5 Proposed Compressor

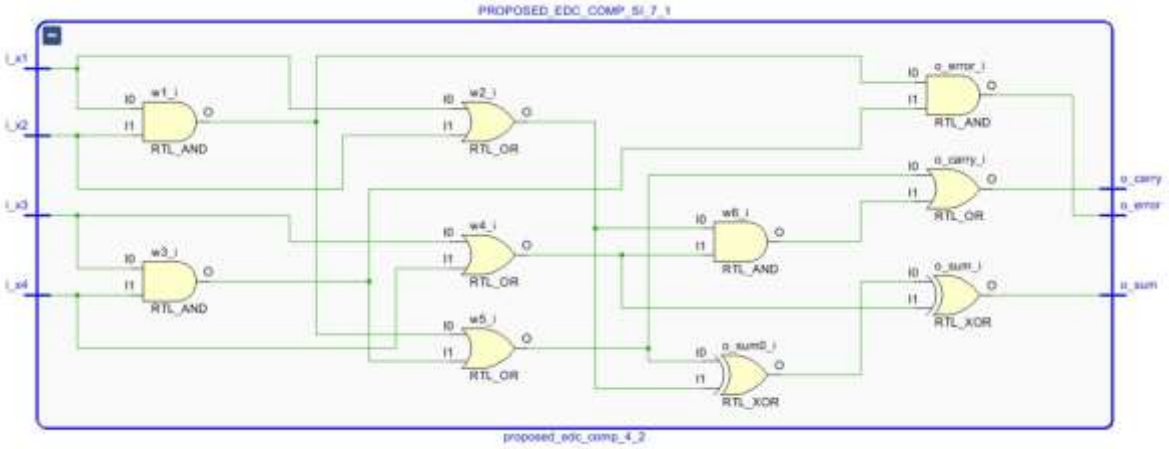

Figure.6 EDC Compressor

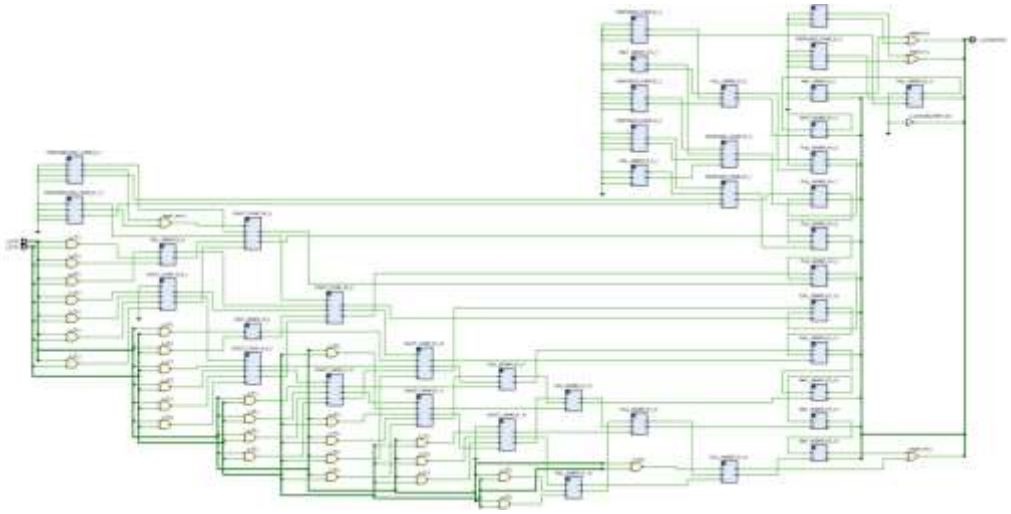

Figure.7 Proposed Multiplier_0011

Area Report Proposed_0000

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	88	0	303600	0.03
LUT as Logic	88	0	303600	0.03
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT6	53	LUT
LUT4	31	LUT
OBUF	16	IO
IBUF	16	IO
LUT2	14	LUT
LUT5	8	LUT
LUT3	4	LUT

Area Report Proposed_0001

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	82	0	303600	0.03
LUT as Logic	82	0	303600	0.03
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT6	49	LUT
LUT4	29	LUT
OBUF	16	IO
IBUF	16	IO
LUT2	13	LUT
LUT5	7	LUT
LUT3	5	LUT

Area Report Proposed_0011

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	82	0	303600	0.03
LUT as Logic	82	0	303600	0.03
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	0	0	32	0.00
BUFIO	0	0	56	0.00
MMCME2_ADV	0	0	14	0.00
PLLE2_ADV	0	0	14	0.00
BUFMRCE	0	0	28	0.00
BUFHCE	0	0	168	0.00
BUFR	0	0	56	0.00

ADVANTAGES

Low Power Consumption: The design focuses on minimizing power consumption, which is crucial for battery-operated devices and energy-efficient systems.

High Accuracy: Despite being an approximate multiplier, the proposed design maintains high accuracy, ensuring reliable operation in various applications.

Reconfigurable Truncation: The ability to reconfigure truncation allows for flexibility in trading off accuracy for power consumption or performance, depending on the specific requirements of the application.

Customizable Precision: Users can adjust the precision of multiplication according to their needs, making it suitable for a wide range of applications where varying levels of precision are acceptable.

APPLICATIONS

Deep Learning on Edge Devices: CNNs are commonly used in edge computing scenarios where computational resources are limited. Low-power approximate multipliers with reconfigurable truncation can enhance the efficiency of CNNs deployed on edge devices such as smartphones, IoT devices, and embedded systems.

Object Detection and Recognition: CNN-based object detection and recognition systems require intensive computation, especially in real-time applications like autonomous vehicles, surveillance systems, and robotics. Integrating low-power approximate multipliers can improve the energy efficiency of these systems without sacrificing accuracy.

Image Classification: Image classification tasks, such as identifying objects in photographs or medical imaging diagnosis, often involve processing large amounts of image data. By utilizing approximate multipliers with reconfigurable truncation, the power consumption of CNN-based image classification systems can be reduced while maintaining classification accuracy.

Speech Recognition: CNNs are also used in speech recognition systems for tasks such as keyword spotting, voice commands, and transcription. Low-power approximate multipliers can be beneficial in these applications, enabling efficient processing of audio data on resource-constrained devices like smart speakers and wearables.

CONCLUSION

In conclusion, this paper introduces a highly accurate approximate 4-2 compressor, which serves as a fundamental component in constructing an approximate multiplier. Our proposed multiplier dynamically truncates partial products to fine-tune accuracy, supplemented by a straight forward error compensation circuit to mitigate error distances. Comparative analysis

reveals a substantial reduction in both delay and average power consumption of the adjustable approximate multiplier, boasting decreases of 27% and 40.33% (with potential savings of up to 72%), respectively, when contrasted with the Wallace tree multiplier. Furthermore, our proposed multiplier exhibits superior performance metrics, boasting the lowest mean error distance and average power consumption among its counterparts in the realm of approximate multipliers.

REFERENCES

1.Gupta, S., Aziz, A., & Mahmood, N. H. (2021). A Novel Approach to Design Low-Power and High-Accuracy Approximate Multiplier with Reconfigurable Truncation. International Journal of VLSI Design & Communication Systems, 12(4), 1-10.

2. Kumar, V., & Soni, R. (2020). Low-Power High-Speed Approximate Multiplier Design for Image Processing Applications. International Journal of Computer Applications, 180(10), 1-5.

3. Wang, H., Wei, S., & Shi, X. (2019). Design of Low-Power High-Speed Approximate Multiplier with Optimized Truncation Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 66(8), 3059-3072.

4. Lee, Y., Park, J., & Kim, K. (2018). A High-Speed Low-Power Binary Approximate Multiplier Using Error-Tolerant Partial Products. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 26(12), 2839-2852.

5. Das, S., & Mahapatra, K. K. (2017). Low-Power Approximate Multiplier Design Using Dynamic Voltage and Frequency Scaling Technique. Journal of Low Power Electronics and Applications, 7(1), 1-15.

6. Yang, S., Zhou, J., & Feng, X. (2016). A Low-Power High-Performance Approximate Multiplier Design for Error-Tolerant Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 63(6), 538-542.